

IN THE SPECIFICATION

Please replace the Abstract with the following replacement Abstract:

ABSTRACT OF THE DISCLOSURE

A digital signal processor configured to perform a Viterbi algorithm includes an instruction fetching unit that fetches instructions and a decoding unit that decodes the instructions fetched by the instruction fetching unit. The digital signal processor also includes an execution unit that executes the instructions decoded by the decoding unit. The execution unit includes an arithmetic logic unit configured to perform a register-register arithmetic logic operation. The arithmetic logic unit compares a first data with a second data, in parallel with a comparison of a third data with a fourth data, and the execution unit outputs new path metrics. Each of the first data, the second data, the third data, and the fourth data is one of four results obtained by adding one of two path metrics to one of two branch metrics.